Packaging, Interconnects and Optoelectronics for the Design of Parallel Computers Workshop

March 18-19, 1992

Hyatt Regency Woodfield, Schaumburg, IL

Scope:

The use of multiprocessors in computing systems and the need for higher speeds have prompted the advent of advanced interconnect technologies. Presently, the clock rates of high-speed computers are limited by interconnection delays rather than device speed, and interconnect and packaging issues will play an increasingly important role in the implementation of computer systems. More specifically, the choice of a given machine architecture will be strongly determined by packaging and interconnect considerations. Multichip modules (MCM) are emerging as an attractive packaging solution with design advantages such as cost and reliability. Optical interconnections have provided higher speed and connectivity in computing applications. The successful implementation of these technologies into high-performance computers requires an understanding of the fundamental interconnect limitations and their relations to machine architecture.

Committee Members:

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Workshop Objective:

The objective of the meeting is to convene researchers, manufacturers, technologists and designers involved in packaging, optoelectronics and computer architecture. Invited speakers will address issues pertaining to machine organization, routing, partitioning, electromagnetic compatibility, clock delay, interconnect modeling and simulation, computer-aided design (CAD) tools, optical interconnects, optoelectronic devices and multichip modules. Problems associated with these issues and their effects on machine performance will be assessed, from which research priorities will be determined for the academic and industrial environments. It is expected that this meeting will help increase the communication between the computer, packaging and optoelectronics communities and make available the information critical to future research directions.

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